AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 1, line 13, and continuing to page 1, line 26, as follows:

Modern wireless communications systems relay on the use of complex digital modulation schemes and multiple carriers to fulfill the requirements of high data transmission capacity over a minimal frequency spectrum. As a consequence, the amplified RF signal to be transmitted and received has usually a complex and strongly time-varying envelope. This complex signal behavior may result in different forms of distortion, including adjacent and alternate channel distortion and intermodulation distortion (IMD). For digital communications system IMD is a large problem since IMD products can be interpreted by the digital system as payload signals. Thus, stringent linearity requirements are imposed on the RF power amplifier and its including elements to suppress the IMD products. A commonly applied technique to improve the linearity of the power amplifier is to apply a biasing signal so that the transistors of the amplifier ~~is~~ are caused to operate in a more linear portion of their available operation range.

Please amend the paragraphs beginning at page 2, line 30, and continuing to page 4, line 5, as follows:

The technology disclosed herein~~present invention~~ overcomes these and other drawbacks of the prior art arrangements.

~~It is a general object of the present invention to~~The technology disclosed herein provides a dynamic biasing of an amplifier and of transistors in the amplifier.

The technology disclosed herein~~It is another object of the invention to~~ also provides a dynamic biasing that reduces intermodulation distortion (IMD) for the amplifier.

The technology disclosed herein ~~Yet another object of the invention is to~~ further provides a dynamic biasing that enables automatic change of operation class for the transistors.

The technology disclosed herein yet further ~~Still another object of the invention is to~~ provides a dynamic biasing that can be applied to an amplifier used in modern wireless communications systems and implemented with a simple circuitry solution.

~~These and other objects are met by the invention as defined by the accompanying patent claims.~~

Briefly, the technology disclosed herein~~present invention~~ involves a dynamic biasing of an amplifier comprising transistors and an associated dynamic bias circuit. The amplifier of an example embodiment~~the invention~~ includes at least two interconnected transistor that are provided for processing, e.g. serially (cascade connection), parallely (parallel connection) or serially and parallely, an input signal. The dynamic bias circuit is connected to the output electrode of a first or driver transistor. In operation when the input signal is applied to, at least, the driver transistor this bias circuit is arranged for detecting a resulting direct current (DC) signal on the output electrode of the driver transistor. In a preferred embodiment of the invention, this DC signal is a DC current signal, e.g. DC drain current signal for a driver transistor of FET (field effect transistor) type. The bias circuit generates a dynamic bias signal, e.g. DC voltage or current signal, based on this detected DC current. The generated bias signal is then applied to the input electrode of a second or final transistor, and a dynamic biasing thereof is obtained.

In a preferred example embodiment ~~of the invention,~~ the dynamic bias circuit detects the DC signal as a voltage drop. In such a case, the DC current is provided to a voltage drop generating element, such as a resistor, and an operation amplifier, transistor or other voltage drop detecting circuitry then detects the resulting voltage drop caused by the DC current running through the resistor.

Please amend the paragraph beginning at page 4, line 14 and continuing to page 4, line 24, as follows:

Generating a dynamic bias signal for the final transistor based on the DC current for the output electrode of the driver transistor (and, thus on the input power) enables a

reduction of the intermodulation distortion for the amplifier and the final transistor. Thus, the bias signal causes the final transistor to operate at a minimum IMD and the linearity of the amplifier increases. Furthermore, dynamically adjusting the bias signal for the final transistor according to the technology disclosed herein~~present invention~~, makes it is possible to automatically change operation class for this transistor. Thus, properties from different operation classes can be obtained by the technology disclosed herein~~invention~~ and the final transistor can be caused to operate in a transistor operation class that presently is most suitable.

Please amend the paragraph beginning at page 4, line 32, and continuing to page 5, line 12, as follows:

The dynamic bias circuit of the technology disclosed herein~~invention~~ can be applied to several amplifier designs and transistor circuits, including serial and parallel combinations of transistor, where a first (driver) transistor is controlling at least a second (final transistor). The amplifier can also comprise additional transistors that participate in the processing of the input signal. In such a case, the dynamic bias circuit can be arranged in an amplifier comprising both serially and parallely connected transistors. The bias signal can be generated based on the DC output current of any transistor in the amplifier, but it is preferred to use the DC current of at least one of the driver transistors. Similarly, the bias signal can be applied to any transistor in the amplifier, but it is preferred to provide it to at least one of the final transistors since these in most cases contribute mostly to the IMD. Thus, the dynamic bias circuit can be connected to transistors in a general amplifier stage, but is particularly adapted for usage in connection with the final amplifier stage of an amplifier

Please amend the paragraphs beginning at page 5, line 21, and continuing to page 5, line 31, as follows:

The technology disclosed herein~~invention~~ offers the following example advantages:

- Reduces and suppresses IMD;
- Increases the linearity of the amplifier;
- Enables automatic change of operation class for a transistor;
- Can be implemented by a simple circuitry solution;
- Can be applied to different amplifier designs and transistor types; and
- Can be used in modern high-frequency wireless communications systems.

Other advantages offered by the technology disclosed herein~~present invention~~ will be appreciated upon reading of the below description of the example embodiments ~~of the invention~~.

Please amend the paragraph beginning at page 6, line 6, and continuing to page 6, line 7, as follows:

Fig. 1 is a schematic diagram of an embodiment of a power amplifier with a dynamic bias circuit according to the present invention;

Please amend the paragraphs beginning at page 6, line 21, and continuing to page 7, line 6, as follows:

Fig. 6 is an illustration of another example embodiment of a power amplifier with a dynamic bias circuit ~~according to the present invention~~;

Fig. 7 is an illustration of yet another example embodiment of a power amplifier with a dynamic bias circuit ~~according to the present invention~~;

Fig. 8 is a detailed diagram of the power amplifier of Fig. 5;

Fig. 9 is a schematic diagram of another example embodiment of a power amplifier with a dynamic bias circuit ~~according to the present invention~~;

Fig. 10 is a schematic diagram of yet another example embodiment of a power amplifier with a dynamic bias circuit ~~according to the present invention~~;

Fig. 11 is flow diagram illustrating ~~the~~ an example method of dynamically biasing a power amplifier ~~according to the present invention~~; and

Fig. 12 is a flow diagram illustrating additional steps of the method of dynamically biasing a power amplifier ~~according to the present invention~~.

Please amend the paragraphs beginning at page 7, line 12 and continuing to page 7, line 21, as follows:

The technology disclosed herein~~present invention~~ relates to dynamic biasing of transistors in an amplifier in order reduce or suppress intermodulation distortion (IMD) and increase the linearity of the amplifier.

Generally, for a given output or input power level of an amplifier a bias signal can be adjusted and applied to improve IMD, i.e. reduce IMD. Since the output and input power are time-dependent the bias signal should follow this power change. The technology disclosed herein~~present invention~~ provides a dynamic bias circuit for use in amplifiers that is able to generate a bias signal based on the input (and output) power level of the amplifiers.

Please amend the paragraph beginning at page 7, line 27, and continuing to page 8, line 31, as follows:

Fig. 1 is a schematic diagram of an embodiment of a power amplifier 1 or amplifier stage with a dynamic bias circuit 100 according to the technology disclosed herein~~present invention~~. By way of example, the power amplifier 1 could for example be used to implement the last two amplifier stages of a radio frequency (RF) transmitter (not illustrated) e.g. in a mobile unit (not illustrated).

The amplifier 1 includes two transistors, exemplified as two general FETs (field effect transistors) 10, 20, interconnected in series in order to process in an input (RF) signal. The transistors 10, 20 could independently be of any FET design, such as JFET (junction FET), IGFET (insulated gate FET), MESFET (metal semiconductor FET) or MOSFET

(metal oxide semiconductor FET). Furthermore, other types of transistors, including bipolar transistors could replace the first FET 10 and/or second FET 20. In the following the technology disclosed herein~~invention~~ will be described and disclosed with reference to amplifier designs including FETs. However, any of the disclosed transistors could readily be exchanged by another transistor type.

The first FET or driver transistor 10 comprises a gate 12, source 14 and drain 16 electrode. The gate or input electrode 12 is adapted for receiving an input (RF) signal and is, in operation, connected to a RF signal source, schematically illustrated as an input terminal 2 in the figure. During operation, the source electrode 14 of the driver transistor 10 is connected to a conductor 6 for receiving a reference voltage level, for example ground reference voltage level. Correspondingly, the drain electrode 16 is arranged for connection with a supply voltage source or terminal 3. This drain or output electrode 16 is further connected to a gate electrode 22 of the second FET or final transistor 20. Similarly to the driver transistor 10, the source 24 and drain 26 electrodes of the final transistor 20 are connected to the conductor 6 and a supply voltage source or terminal 4, respectively. It is anticipated ~~by the invention,~~ that the two terminals 3 and 4 could be connected to a common supply voltage, especially if the driver 10 and final 20 transistor is of a same type. Once the input (RF) signal is provided on the input terminal 2, the driver transistor 10 processes (amplifies) this signal and outputs an intermediate alternating current (AC) signal on its drain (output) electrode 16. This intermediate AC signal is brought to the gate (input) electrode 22 of the final transistor 22, which processes the signal and outputs a processed (amplified) RF output signal at an output terminal 5 connected to its drain electrode 26.

Please amend the paragraph beginning at page 9, line 15, and continuing to page 11, line 24, as follows:

In the power amplifier of Fig. 1, the (drain) current of the driver 10 and final ~~10~~ transistor follows the input power level. In addition, by monitoring the current (DC current signal) of the driver stage 10, the output power level therefrom can be detected. This output

power level of the driver stage 10 provides knowledge of the output power level of the final transistor 20 and, thus, of the amplifier 1. As a result, the bias of the final transistor 20 can be adjusted for a given input and output power level to continuously obtain the best IMD performance. Furthermore, the linearity of the amplifier 1 is increased be generating and applying an optimal dynamic bias signal.

Fig. 2 is a diagram schematically illustrating IMD for a general transistor at different input or output power levels for the transistor. The IMD curve 300 generally has local maximum point at lower power levels. Increasing the power beyond this maximum point decreases the IMD curve 300 and it eventually reaches a minimum point 310. However, if the power increases further it will result in compression of the transistor and IMD increases dramatically. Thus, the optimal operation of the transistor in view of IMD is to operate the transistor at, or at least close to, the minimum IMD point 310. Generating a dynamic bias signal according to the technology disclosed herein~~invention~~ and applying it to the transistor enables movement of this minimum point 310 to different power levels, schematically illustrated by a dotted line 320. Thus, the transistor is caused to preferably continuously operate at, or close to, the minimum IMD point 310, regardless of the current input or output power level. In other words, the applied bias signal enables the transistor to almost always operate at this minimum IMD.

Dynamic adjustment of the bias signal for the final transistor according to the technology disclosed herein~~present invention~~ makes it also possible to automatically change operation class for this transistor. Thus, properties from different operation classes can be obtained by the technology disclosed herein~~present invention~~. As the person skilled in the art knows, a class A transistor operation is characterized by a large applied bias and good IMD performance and linearity. However, a major drawback is that the DC current consumption is high and the efficiency is low, in particular in back-off conditions. Prolonged operation with high current consumption and low efficiency may be a problem especially when the amplifier is arranged in a mobile unit with a limited energy supply (powered by batteries). Class AB, B and C operation have better efficiency but at the cost of

worse IMD, in particular for higher output power levels. By dynamically adjusting and applying a bias signal generated according to the technology disclosed herein~~present invention~~, the final transistor can be caused to operate in a transistor operation class that presently is most suitable. The actual choice of operation class may be changed based on input or output power level. Thus, by generating a bias signal that is based on the DC current signal of the driver transistor, which in turn is proportional to the input power of the RF signal, the operation class can be changed for different input power levels.

Fig. 3 is an illustration showing a possible implementation of the dynamic bias circuit 100 according to the technology disclosed herein~~present invention~~. In ~~this figure,~~Fig. 3 the bias circuit 100 is realized as a voltage drop generator 130 and a voltage drop detector 140. The voltage drop generator could be a resistor 130 or any other resistance element that generates a voltage drop due to the DC current of the driver transistor 10 passing therethrough. An example of such another resistance element is a tapered metal, e.g. copper, wire. This resistor 130 has a first end connected to the drain electrode 16 of the driver transistor 10 and a second end connected to the supply voltage terminal 3. The voltage drop detector, exemplified as an operator amplifier 140 in the Fig. 3~~figure~~, is arranged for detecting the generated voltage drop as a voltage difference on its two input terminals 142, 144. The first input terminal 142 is connected to the drain 16 of the driver transistor 10 (and the first end of the resistor 130), whereas the second input terminal 144 is coupled to the voltage terminal 3 (and the second end of the resistor 130). Thus, the input voltage of terminal 142 is $V_{supply} - R_{130}I_d$, where V_{supply} is the supply DC voltage of terminal 3, R_{130} is the resistance value of the resistor 130 and I_d is the (DC) drain current. The corresponding input voltage of terminal 144 is simply the supply voltage level V_{supply}. The operation amplifier 140 then generates the dynamic bias signal based on the voltage difference and applies it, as a bias DC voltage signal, through its output terminal 146 to the gate electrode 22 of the final transistor 20. Thus for this embodiment, a change in the input power of the RF signal results in a change in the DC drain current of the driver transistor 10. This current

change affects the voltage drop proportionally and, thus, the output voltage of the operator amplifier 140. As a result, an efficient dynamic biasing of the final transistor 20 is obtained.

In Fig. 3~~the figure~~ the operation amplifier 140 has been provided with a single voltage supply illustrated by voltage terminal 7 and the ground level. However, also a symmetric or unsymmetric supply voltage is possible.

Please amend the paragraphs beginning at page 12, line 4, and continuing to page 12, line 18, as follows:

The resistor 130 and operation amplifier 140 of the dynamic bias circuit 100 in Fig. 3 can be exchanged ~~to~~ for any other DC current detecting element or circuitry. There are several dedicated or adapted, often operation amplifier based, circuits for DC current detection known in the art, including current sensing integrated circuits (ICs). Any such circuit could then be included in the bias circuit 100 of the technology disclosed herein~~present invention~~ for current detection and possibly bias signal generation purposes.

Another possible implementation of the dynamic bias circuit 100 of the technology disclosed herein~~invention~~ is illustrated in Fig. 4. This bias circuit 100 is similar to the circuit discussed above in connection with Fig. 3 except that the operation amplifier (voltage drop detector) has been exchanged by a bipolar transistor 150. However, this bipolar transistor 150 generally performs the same functionality as the operation amplifier of Fig. 3, i.e. detects a voltage drop over a resistor 130 caused by the DC drain current of the driver transistor 10.

Please amend the paragraphs beginning at page 13, line 7, and continuing to page 13, line 28, as follows:

Depending on the actual choice of second or final transistor in Figs. 3-4, the bias signal generated by the operation amplifier or transistor may be sufficient for efficient biasing of the final transistor. However, in some applications it is preferred to e.g. amplify or otherwise adjust the bias signal before applying it to the final transistor. This is particular

the case if the final transistor is a bipolar transistor or a large FET transistor, and thus requires a fairly large bias signal for efficient operation. In such a case, it may be possible that the operation amplifier or transistor is unable to directly generate such a large bias signal. This is solved by ~~the invention by~~ introducing bias signal processing or amplifying elements or circuitry in the dynamic bias circuit, which is exemplified in Fig. 5.

The power amplifier 1 of ~~this~~ Fig. 5 corresponds to the amplifier of Fig. 3 with addition of a bias signal amplifying transistor 160. The transistor 160, here exemplified by a bipolar transistor, has a base electrode connected to the output terminal 146 of the operation amplifier 140. The collector is connected to the conductor or ground level, whereas the emitter electrode is coupled to three resistors~~transistors~~ 162, 164 and 166. The two resistors 162, 164 forms a voltage divider that provides, together with the supply voltage source or terminal 8, an emitter bias. The third resistor 166 is coupled to the gate electrode 22 of the final transistor 20. The functionality of this resistor 166 corresponds to resistor 156 of Fig. 4, i.e. it serves as an AC signal blocking element.

Please amend the paragraph beginning at page 14, line 12, and continuing to page 14, line 29, as follows:

The technology disclosed herein~~present invention~~ is not limited to an amplifier comprising a driver transistor and a single final transistor. Fig. 6 illustrates a power amplifier 1 including a driver transistor 10 driving two parallel final transistors 20, 30. The amplifier 1 also comprises a dynamic bias circuit 100 according to the technology disclosed herein~~present invention~~, here illustrated by a voltage drop generating resistor 130, operation amplifier 140 and two bias signal amplifying transistors 160, 170. Correspondingly to the first final transistor 20, a second final transistor 30 has a gate electrode 32 connected to the output drain electrode 16 of driver transistor 10 and adapted for receiving the intermediate AC signal therefrom. The source electrodes 24, 34 of the final transistors 20, 30 are connected to the ground level or conductor, whereas their respective drain electrodes 26, 36 are coupled to supply DC voltage terminals or sources 4A, 4B and to output terminals 5A,

5B. It is anticipated by the invention that the two supply voltage terminals 4A, 4B may be interconnected, i.e. provide one and the same supply voltage to the two final transistors 20, 30, especially if the transistors 20, 30 are of a same type. In addition, the power amplifier 1 could provide two, possibly different, output RF signals via output terminal 5A, 5B. However, these terminals 5A, 5B could be interconnected to output a single RF signal.

Please amend the paragraph beginning at page 15, line 22, and continuing to page 15, line 32, as follows:

In the preceding Figs. 1 and 3-6, the power amplifier has been illustrated as a two-step amplifier with a single driver transistor cascade connected to one or several final transistors. Fig. 7 illustrates another possible power amplifier design according to the technology disclosed herein~~present invention~~. This amplifier 1 comprises three cascaded transistors 10, 20 and 40 and a dynamic bias circuit 100. A first driver transistor 10 is adapted for receiving an input RF signal and for generating a first intermediate AC signal. This AC signal is applied to a gate electrode 42 of a second driver transistor 40 that processes the signal and outputs a second intermediate AC signal at its drain electrode 46. This second AC signal is applied to the final transistor 20, which generates an output RF signal.

Please amend the paragraphs beginning at page 18, line 16, and continuing to page 19, line 16, as follows:

The dynamic bias circuit according to the technology disclosed herein~~present invention~~ has hitherto been described and disclosed with reference to an amplifier or amplifier stage comprising cascade connected transistors. However, the technology disclosed herein~~invention~~ is not limited to such amplifier designs. The bias circuit can also be applied to other transistor connections employed in the art, such as parallel transistor connections and combinations of parallel and serial connections. A general transistor connection design, to which the teaching of the technology disclosed herein~~present~~

~~invention~~ can be applied, comprises at least two interconnected transistor adapted for processing, e.g. serially (cascade connection), parallelly (parallel connection) or serially and parallelly, an input signal.

Fig. 9 is a schematic diagram of an example embodiment of a power amplifier 1 with a dynamic bias circuit according to the technology disclosed herein~~present invention~~. This power amplifier 1 comprises two parallel-connected transistors 10, 20. The gate electrodes 12, 14 of the transistors 10, 20 are connected for, in operation, receiving an input RF signal from an input signal terminal or source 2. The source electrodes 14, 24 are connected to a reference voltage level, e.g. ground. The drain electrodes 16, 26 are in connection with voltage supply sources, represented as two different terminals 3, 4 in the figure, but can be realized as a single common supply terminal. Furthermore, the drain electrodes 16, 26 are coupled to an output terminal 5 for providing a processed (amplified) output RF signal.

A dynamic bias circuit 100 according to the technology disclosed herein~~invention~~ is arranged in the amplifier 1 for detecting the DC (drain) current signal of the first transistor 10. Thus, the bias circuit 100 is connected between the voltage supply terminal 3 and the drain electrode 16 of the transistor 10. As was discussed in connection with Fig. 1, the bias circuit 100 comprises a bias generator 110 for generating a bias signal based on the DC drain current, e.g. as determined based on a detected voltage drop caused by the drain current. The bias signal is then provided by a bias applier 120 to the gate (input) electrode of the second transistor 20. In other words, a dynamic biasing of this second transistor 20 based on the DC drain current and, thus, the power of the input RF signal is obtained. This dynamic biasing enables efficient operation of the transistor 20 and the amplifier 1 by suppressing the IMD for this transistor 20.

Please amend the paragraphs beginning at page 20, line 8, and continuing to page 21, line 20, as follows:

A dynamic bias circuit 100 is connected to the drain 14 of the first transistor 10 for generating a bias signal based on the DC drain current of this transistor 10. In a first embodiment of the amplifier 1, the generated bias signal could then be applied by the bias applier 120 to the input (gate) electrodes 22A, 22B of the final transistors 20A, 20B in order to get a dynamic biasing and IMD suppression according to the technology disclosed hereinpresent invention. In a second embodiment, the bias signal is also applied to the gate 52 of the second driver transistor 50.

The power amplifiers of Figs. 9 and 10 have been schematically disclosed in respective figure. It is anticipated by the invention that additional components, elements and circuitry could be added to the amplifiers giving a corresponding more detailed implementation as is illustrated in Fig. 8 for a cascaded transistor design. Generally, although not depicted, the amplifier circuitry as well as the dynamic bias circuitry discussed above and disclosed in Figs. 1 and 3 to 10 may include any number of active diodes, additional capacitors and resistors in the final design as long as the basic operation of the dynamic bias circuit is not jeopardized. In addition, in operation, the dynamic bias circuit may be combined with other circuitry that may impact bias control to compensate for temperature, gain or other operation aspects.

Fig. 11 is a flow diagram illustrating the method of dynamically biasing an amplifier comprising at least two interconnected transistors according to the technology disclosed hereinpresent invention. The method generally starts in step S1, where an input (RF) signal is applied to an input electrode of at least one of the transistors. A resulting DC signal, i.e. DC current signal, of the output electrode of at least a first (driver) transistor receiving the input signal is detected in step S2. A bias signal, e.g. DC voltage or current bias signal, is then generated in step S3 based on the detected DC signal. Due to the relation between the arising DC current signal and the power level of the input (RF) signal, the bias signal will be based on this input power. The generated bias signal is subsequently applied to, in step S4,

an input electrode of at least a second (final) transistor for dynamically biasing the transistor and affecting the operation thereof in order to reduce IMD. The method then ends.

Fig. 12 is a flow diagram illustrating the DC signal detecting step of Fig. 11 in more detail and an additional step of the biasing method of the technology disclosed hereininvention. The method continues from step S1 of Fig. 10. In a next step S21, the resulting DC current signal is applied to a resistance element in order to generate a voltage drop thereover. Step S22 detects this arising voltage drop and the next step S3 generates a bias signal that depends on, e.g. proportional to, the detected voltage drop. The bias signal is then optionally amplified or otherwise adjusted in step S31 before application to the second transistor in step S4 of Fig. 11. This amplification or adjustment is preferably performed so that the bias signal becomes adjusted for the particular transistor, to which it is applied.